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EXAMINER	
POOS, JOHN W	

ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
10/17/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/554,970	HOESS, WOLFGANG	
	Examiner	Art Unit	
	JOHN W. POOS	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/26/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6, 9-12 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Asazawa et al. (US 5,844,437).

In regard to Claim 1 (as taught in Figure 3):

A flip-flop circuit arrangement, comprising:

a pair-of input terminals to provide a differential clock signal; (C, C(bar))

a pair of output terminals to provide a differential output signal, (Q, Q(bar))

differential amplifiers each of the differential amplifiers comprising at least two transistors ((Q11 and Q12), (Q13 and Q14), (Q21 and Q22), (Q23 and Q24)), the transistors comprising collectors, each collector being part of one of plural series circuits containing a resistor ((R11, R12, and R13) and (R21, R22, and R23)), the series circuits being positioned between a power supply potential terminal (Vcc) and a first shared emitter node (emitters of Q11-Q14) and/or a second shared emitter node (emitters of Q21-Q24), sets of the collectors being interconnected (M, M(bar) and Q, Q(bar) nodes) to form a D flip-flop structure, the output terminals being at an output of at least one differential amplifier (Q, Q(bar), the output of differential amplifier composed of Q23 and Q24));

a first current source to connect the first shared emitter node to a reference potential terminal; (IS11)

a second current source to connect the second shared emitter node to the reference potential terminal; (IS21)

a first switch (Q71) connected to the power supply potential terminal (Vcc through R52) and connected to the first shared emitter node, the first switch having first control terminal that comprises part of the input terminals; (Q71, input terminal C, where the switch and emitters are commonly connected to Vss via the current sources)

a second switch (Q72) connected to the supply potential terminal (Vcc through R61) and connected to the second shared emitter node, the second switch having a second control terminal that comprises part of the input. (Q72, input terminal C(bar), where the switch and emitters are commonly connected to Vss via the current sources)

In regard to Claim 2 (as taught in Figure 3):

The flip-flop circuit of claim 1, wherein the differential amplifiers comprise:

a first differential amplifier (Q13 and Q14), comprising a first pair of emitter- coupled transistors connected to the first shared emitter node, the first pair of emitter-coupled transistors comprising collector terminals that form at least parts of a first circuit node and a second circuit node, the first pair of emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals;

a second differential amplifier (Q11 and Q12), comprising a second pair of emitter-coupled transistors connected to the second shared emitter node, the second pair of emitter-coupled transistors comprising collector terminals that are connected to the first circuit node and/or to the second circuit node, the second pair of emitter-coupled transistors comprising base terminals that form at least part of a third circuit node and a fourth circuit node;

a third differential amplifier (Q23 and Q24), comprising a third pair of emitter- coupled transistors connected to the second shared emitter node, the third pair of emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the third pair of emitter- coupled transistors comprising and whose base terminals that are cross-connected to collector terminals; and

a fourth differential amplifier (Q21 and Q22) comprising a fourth pair of emitter-coupled transistors connected to the first shared emitter node, the fourth pair of emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the fourth pair of emitter-coupled transistors comprising base terminals that are connected to the second circuit node and/or to the first circuit node.

In regard to Claim 3 (as taught in Figure 3):

The flip-flop circuit of claim 2, wherein the first, the second, the third, and the fourth circuit nodes are each connected via a resistor in a series circuit to the power supply potential terminal. (R11, R12, R13, R21, R22, R23)

In regard to Claim 4:

The flip-flop circuit claim 2, wherein the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using bipolar circuit technology. (Figure 3 and Asazawa Column 7: lines 5-10)

In regard to Claim 6 (as taught in Figure 3):

The flip-flop circuit of claim 1, wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology. (Q11-Q14 have coupled emitters, as well as Q21-Q24)

In regard to Claim 9:

A flip-flop circuit comprising:

input terminals to provide a clock signal; (C, C(Bar))

output terminals to provide an output signal, (Q, Q(bar))

a first differential amplifier (Q13, Q14) comprising first emitter-coupled transistors having emitters connected to a first emitter node, the first emitter-coupled transistors comprising collector terminals that form at least parts of a first circuit node and a second circuit node, the first emitter-coupled transistors comprising base terminals that are cross-connected to collector terminals of the first emitter-coupled transistors;

a second differential amplifier (Q11, Q12) comprising second emitter-coupled transistors having emitters connected to a second emitter node, the second emitter-coupled transistors comprising collector terminals that are connected to the first circuit node and/or to the second circuit node, the second emitter-coupled transistors comprising base terminals that form at least part of a third circuit node and a fourth circuit node;

a third differential amplifier (Q23, Q24) comprising third emitter-coupled transistors having emitters connected to the second emitter node, the third emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth circuit node, the third emitter-coupled transistors comprising base terminals that are cross-cormected to collector terminals of the third emitter-coupled transistors; and

a fourth differential amplifier (Q21, Q22) comprising fourth emitter-coupled transistors having emitters connected to the first emitter node, the fourth emitter-coupled transistors comprising collector terminals that are connected to the third circuit node and/or to the fourth

circuit node, the fourth emitter-coupled transistors comprising base terminals that are connected to the second circuit node and/or to the first circuit node;

a reference potential that is connectable to the first emitter node and to the second emitter node; (Vss)

a first switch (Q71) connected to the power supply potential terminal (Vcc through R52) and connected to the first shared emitter node, the first switch having first control terminal that comprises part of the input terminals; (Q71, input terminal C, where the switch and emitters are commonly connected to Vss via the current sources)

a second switch (Q72) connected to the supply potential terminal (Vcc through R61) and connected to the second shared emitter node, the second switch having a second control terminal that comprises part of the input. (Q72, input terminal C(bar), where the switch and emitters are commonly connected to Vss via the current sources)

In regard to Claim 10 (as taught in Figure 3):

The flip-flop circuit of claim 9, wherein the first, the second, the third, and the fourth circuit nodes are each connected via a resistor in a series circuit to the power supply potential terminal. (R11, R12, R13, R21, R2, R23).

In regard to Claim 11:

The flip-flop circuit of claim 9, wherein the first, the second, the third, and the fourth differential amplifiers and the first and the second switches are implemented using bipolar circuit technology. (Figure 3 and Asazawa Column 7: lines 5-10).

In regard to Claim 12 (as taught in Figure 3):

The flip-flop circuit of claim 9, further comprising:

a first current source to connect the first emitter node to the reference potential terminal; and (IS11)

a second current source to connect the second emitter node to the reference potential terminal. (IS21)

In regard to Claim 14 (as taught in Figure 3):

The flip-flop circuit of claim 9, wherein the flip-flop circuit is implemented in emitter-coupled logic circuit technology. (Q11-Q14 have coupled emitters, as well as Q21-Q24)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asazawa et al. (US 5,844,437).

In regard to Claim 7:

All of the claim limitations have been discussed with respect to Claim 1 above, except for a shift register comprising the flip-flop circuit of claim 1. The examiner takes Official Notice that it is old and notoriously well known to form a shift register using flip-flop circuits. Therefore it would have been obvious to one skilled in the art at the time of the invention to use the flip-flop taught by Asazawa in a shift register in order to obtain the benefits/advantages taught by Asazawa, i.e. operating at a low power and a high frequency (Column 4: lines 60-67).

In regard to Claim 15:

All of the claim limitations have been discussed with respect to Claim 9 above, except for a shift register comprising the flip-flop circuit of claim 9. The examiner takes Official Notice that it is old and notoriously well known to form a shift register using flip-flop circuits. It would have been obvious to one skilled in the art at the time of the invention to use the flip-flop taught by Asazawa in a shift register in order to obtain the benefits/advantages taught by Asazawa, i.e. operating at a low power and a high frequency (Column 4: lines 60-67).

6. Claims 5, 8, 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asazawa et al. (US 5,844,437), in view of Tung et al. (US 6,559,693).

In regard to Claim 5:

All of the claim limitations have been discussed with respect to Claim 1 above, except for wherein the first current source and the second current source each comprise a transistor in implemented using metal oxide semiconductor circuit technology. Tung (693) teaches wherein the first current source and the second current source each comprise a transistor in implemented using metal oxide semiconductor circuit technology (Figure 1: MC1, MC2 and Tung Column 3: lines 12-14). It would have been obvious to one skilled in the art at the time of the invention to

use MOSFET technology for the current sources, in order to achieve low operating power consumption and low supply voltage requirements (Tung Column 1: lines 37-38).

In regard to Claim 13:

All of the claim limitations have been discussed with respect to Claims 9 and 12 above, except for wherein the first current source and the second current source each comprise a transistor in implemented using metal oxide semiconductor circuit technology. Tung (693) teaches wherein the first current source and the second current source each comprise a transistor in implemented using metal oxide semiconductor circuit technology (Figure 1: MC1, MC2 and Tung Column 3: lines 12-14). It would have been obvious to one skilled in the art at the time of the invention to use MOSFET technology for the current sources, in order to achieve low operating power consumption and low supply voltage requirements (Tung Column 1: lines 37-38).

Response to Arguments

7. Applicant's arguments filed 7/30/2008 have been fully considered but they are not persuasive.

Applicant's argument is that the switches are not connected to the shared emitter nodes. This is not persuasive because the claim does not require a ***direct*** connection of the switches and shared emitter nodes, and therefore Asazawa's switches are connected to the shared emitters nodes through the current sources and Vss connection.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN W. POOS whose telephone number is (571)270-5077. The examiner can normally be reached on M-F (alternating Fridays off), E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lincoln Donovan can be reached on 571-272-1988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Kenneth B Wells/
Primary Examiner, Art Unit 2816

/J. W. P./
Examiner, Art Unit 2816